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Mail Stop Appeal Brief - Patents Commissioner for Patents P.O. Box 1450

Alexandria, VA 22313-1450

Attorney for Appellants

Date: 16 July 2004

Appl. No.:

09/885,217

Applicant(s):

Keeth, et al.

Filed:

20 June 2001

Title:

256 MEG DYNAMIC RANDOM ACCESS MEMORY

Art Unit:

2816

Examiner:

Anh Quan Tra

Docket No.:

DB000575-012

TRANSMITTAL

To:

Mail Stop Appeal Brief - Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-captioned application, please find the following:

• Appellants' Reply Brief to the Examiner's Answer (in triplicate).

Also enclosed is a return postcard. Please date stamp the postcard and return it to the address thereon in order to acknowledge receipt of the above-mentioned correspondence. The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to our Deposit Account No. 20-0888. A duplicate copy of this Transmittal letter is enclosed.

Respectfully submitted,

Edward L. Pencoske Reg. No. 29,688

Thorp, Reed & Armstrong One Oxford Centre, 14th Floor

Pittsburgh, PA 15219

(412) 394-7789

Attorney for Applicants

Dated: 16 July 2004

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APPELLANTS' REPLY BRIEF TO THE EXAMINER'S ANSWER

In response to the Examiner's Answer mailed 3 June 2004, Appellant respectfully requests entry of the instant Reply for the above-captioned application.

(1) Issues

- (a) Whether independent claim 223 is anticipated by Morishita et al. pursuant to 35 U.S.C. §102 (e). More specifically, does Morishita disclose "an active reference circuit ... for producing a reference signal having a desired relationship with the external voltage... wherein said reference signal is dependent upon said external voltage"?
- (b) Do any of the secondary references (Zarrabian used in a rejection of independent claim 496; Tsay used in a rejection of independent claims 231 and 504; and Hayakawa and Park used in a rejection of independent claim 247) provide the missing teachings?

(2) Argument

(a) Morishita et al. does not disclose "an active reference circuit ... for producing a reference signal having a desired relationship with the external voltage... wherein said reference signal is dependent upon said external voltage."

The Examiner's Answer upheld the rejection of claim 223 pursuant to 35 U.S.C. § 102(e) as being anticipated by Morishita et al. (US Pat. No.: 5,757,175). Specifically, the Examiner states:

As to claim 223, figure 17 of Morishita et al. discloses a voltage reference circuit responsive to an external voltage ($ExtV_{CC}$) for supplying a reference voltage (INV_{CC}), the voltage reference circuit comprising an active reference circuit (VGR) for receiving the external voltage and for producing a reference signal (V_{ref}) having a desired relationship with the external voltage.

Figure 19 shows the active reference circuit (VRG) comprising a current source (TP4) utilizing a current mirror for providing current to a diode stack (CVC) having an adjustable impedance, wherein the reference signal is dependent upon the external voltage. Column 2, lines 17-20, teaches that the reference voltage $V_{\rm ref}$ is independent of the external power supply voltage $EXV_{\rm CC}$ when the voltage $EXV_{\rm CC}$ is at least at a prescribed voltage level. Thus, when the voltage $EXV_{\rm CC}$ is lower than the prescribed voltage level, the reference voltage is dependent of the external supply voltage $EXV_{\rm CC}$).

Figure 17 further shows a unity gain amplifier (CMP, DT) responsive to the reference signal for producing the reference voltage.

It is respectfully submitted that the Examiner has misconstrued the teachings of Morishita. More specifically, the Examiner states that, because Morishita teaches that the reference signal is independent of the external power supply voltage EXV_{CC} when the voltage EXV_{CC} is at least at a prescribed voltage level, the reference signal is dependent upon the external supply voltage EXV_{CC} when EXV_{CC} is lower than a prescribed voltage level. Morishita, however, teaches that the VRG circuit does not begin to generate the reference signal until after EXV_{CC} exceeds a prescribed voltage level. (See column 3, lines 31-45, and column 4, lines 31-47.) Thus, during the time that the reference signal is dependent upon the external voltage (as construed by the Examiner), the reference signal of Morishita cannot have "a desired relationship with the external voltage" because there is no reference signal being produced. Furthermore, during the time that the reference signal is being produced (i.e., when the external supply voltage EXV_{CC} exceeds the prescribed voltage level), the reference signal is independent of the external voltage. (See column 2, lines 16-20 and column 6, lines 12-17.)

In contrast, claim 223 recites "an active reference circuit ... for producing a reference signal having a desired relationship with the external voltage... wherein said reference signal is dependent upon said external voltage." Thus, the produced reference signal of the claimed invention is both dependent upon said external voltage and has a desired relationship with the external voltage. As discussed above, Morishita fails to teach this feature.

Thus, it is believed that claim 223 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 223 pursuant to §102(e) in view of Morishita be withdrawn.

(b) None of the secondary references provides the missing teachings of Morishita.

(1) Claim 496

Claim 496 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over Morishita in view of Zarrabian (US Pat. No.: 5,838,076). Claim 496 recites "a unity gain amplifier responsive to a signal available at the node for producing the reference voltage, wherein said signal is dependent upon said external voltage." It is respectfully submitted that the Office has pointed to no portion of Morishita that teaches a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal, wherein said signal is dependent upon said external voltage. It is respectfully submitted that the Office has not demonstrated that Zarrabian provides this missing teaching. Thus, for the same reasons discussed above in conjunction with claim 223, it is believed that claim 496 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 496 be withdrawn.

(2) Claims 231 and 504

Claims 231 and 504 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Tsay et al (US Pat. No.: 6,127,881) in view of Morishita. As to claims 231 and 504, the Examiner stated:

Tsay's figure 2 shows a multiplier circuit for generating a voltage signal higher than a reference voltage (V_{ref}). Thus, Tsay's figure 2 shows all limitations of the claims except for detail of the reference circuit. [Emphasis added]

Claim 231 recites "an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship to the external voltage, wherein said reference signal is dependent upon said external voltage." Claim 504 recites "a unity gain amplifier responsive to a signal available at the node for producing a reference voltage, wherein said signal is dependent upon said external voltage." As discussed above in conjunction with claims 223 and 496, Morishita fails to teach a voltage reference circuit, either with or without a unity gain amplifier, that produces a reference voltage in response to a reference signal "having a desired relationship to the external voltage, wherein said reference signal is dependent upon said external voltage" and, as stated by the Examiner, Tsay fails to provide this missing teaching. Thus, it is believed that claims 231 and 504 are in condition for allowance.

Accordingly, it is respectfully requested that the rejection of claims 231 and 504 be withdrawn.

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(3) Claim 247

Claim 247 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Hayakawa in view of Tsay, Morishita and Park. Claim 247 recites "producing a reference signal having a desired relationship with the external voltage, wherein said reference signal is dependent upon said external voltage." As discussed above, Tsay and Morishita fail to suggest or teach a voltage reference circuit that produces a reference signal having a desired relationship with the external voltage, wherein said reference signal is dependent upon said external voltage and the Office has not demonstrated that Park or Hayakawa provide the missing teachings. Thus for the same reasons discussed above, it is believed that claim 247 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 247 be withdrawn.

Conclusion

For the reasons set forth above appellant respectfully requests that the rejections of independent claims 223, 231, 247, 496, and 504 be withdrawn and the application be allowed to issue with all of the pending claims, 223, 225 - 237, 247 - 250, 496, and 499 - 515.

Respectfully Submitted,

Edward L. Pencoske Reg. No. 29,688

THORP REED & ARMSTRONG, LLP

One Oxford Centre

301 Grant Street, 14th Floor Pittsburgh, PA 15219

(412) 394-7789

Attorney for Appellants

Dated: 16 July 2004